2. (Amended) The process of claim 1 wherein each of the blocks includes at least one output signal port.

A7 Cont'd

3. (Amended) The process of claim 1 wherein a plurality of input signal values and the output signal values have at least one attribute.

---

14. (Amended) A block diagram modeling process comprising:

A8

providing a first block and a second block, the blocks representing functional entities;

generating a plurality of output signal values from the first and second block;

grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

processing the composite signal in a third block.

---

16. (Amended) The process of claim 14 wherein an input signal is a second composite signal.

A9

17. (Amended) The process of claim 14 further comprising decomposing the composite signal into a plurality of input signal values.

---

21. (Amended) A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:

A10

provide a plurality of blocks, each of the blocks representing functional entities;

generate a plurality of output signal values from the plurality of blocks;

group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

output the first composite signal.

---

25. (Amended) A processor and a memory configured to:

A11

provide a plurality of blocks, each of the blocks representing functional entities;

generate a plurality of output signal values from the plurality of blocks;

group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

output the first composite signal.